

# Revisiting the Security of LPN based RFID Authentication Protocol and Potential Exploits in Hardware Implementations

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- LCMQ<sup>1</sup>: consolidation of LPN, Circulant Matrix and Multivariate Quadratic (MQ) problem

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<sup>1</sup>Z. Li, G. Gong, and Z. Qin, "Secure and Efficient LCMQ Entity Authentication Protocol," IEEE Trans. Information Theory, vol. 59, no. 6, pp. 4042-4054, 2013. 

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  - Demonstrate the use of HTH to induce precise fault attack.
  - Less than  $2^8$  rounds of protocol run to guess the key and forge the authentication

# LPN Problem

- Let  $A$  be a random  $(l \times m)$ -binary matrix
- $\mathcal{K}$  be a random  $m$ -bit vector
- $\epsilon \in (0, \frac{1}{2})$  be a noise parameter
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- **LPN Problem:** Given  $A, \epsilon$ , and  $\mathbf{z} = \langle A \cdot \mathcal{K}^t \rangle \oplus \mathcal{V}^t$ , find a  $k$ -bit vector  $\mathbf{y}^t$  such that  $\text{Hwt}(\langle A \cdot \mathbf{y}^t \rangle \oplus \mathbf{z}) \leq \epsilon \times l$ .

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- This problem is proven to be NP-Hard and the key length  $m$  and the noise level  $\epsilon$  decides the security of the problem instances.
- For 80-bit security,  $m$  and  $\epsilon$  are set to 512 and 0.25.

Given  $n < m$ , a circulant-P2 matrix is an  $(m \times m)$  square circulant matrix, or an  $(n \times m)$  landscape circulant matrix, or an  $(m \times n)$  portrait circulant matrix, satisfying the below criteria.

- 1 It must be a binary matrix.
- 2  $m$  is a prime number such that 2 is a primitive element of the finite field  $\mathbb{F}_m$ . Here,  $m$  is defined as a *P2 number*.
- 3 No row vector and column vector of a Circulant-P2 matrix can be all zeroes or all ones.

$$\textcircled{1} \mathcal{E} = \{\mathbf{a} \mid \mathbf{a} \in \{\{0, 1\}^m \setminus \{\{0\}^m, \{1\}^m\}\} \ \& \ \text{Hwt}(\mathbf{a}) \text{ is even}\}$$

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  - where  $\mathbf{b}_i \in_R \{0, 1\}^m$
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  - $\mathbf{r}_i \in_R \{0, 1\}^{m-n-1}$
  - determine  $\mathbf{K}_1$  and  $\mathbf{K}_2$

# Mapping to Multivariate Quadratic (MQ) Problem

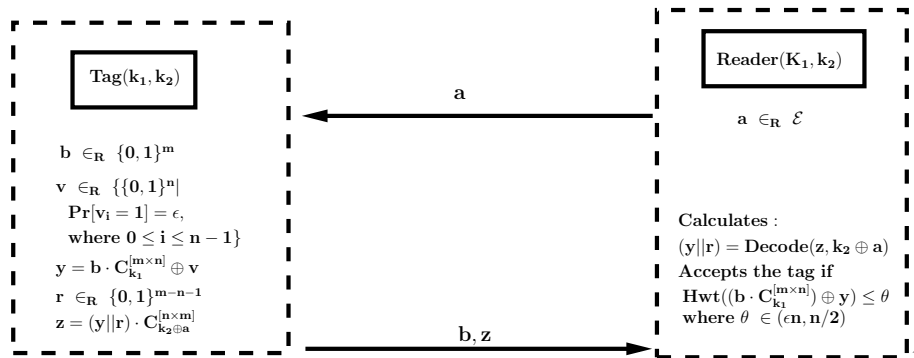
If  $n = m - 1$  and there is no noise, the problem reduces to finding  $K_1$  and  $K_2$  such that:

$$(\mathbf{b}_i \in_R \{0, 1\}^m, \mathbf{z}'_i = (\mathbf{b}_i \cdot C_{\mathbf{K}_1}^{[m \times n]}) \cdot C_{\mathbf{K}_2}^{[(m-1) \times m]})$$

This problem is an instance of MQ problem in  $2(m - 1)$  variants, known to be NP-complete.

**MQ Problem:** Given a system of  $d$  multivariate quadratic equations in  $t$  variables over a finite field, find a valid solution satisfying all equations.

# The LCMQ Protocol



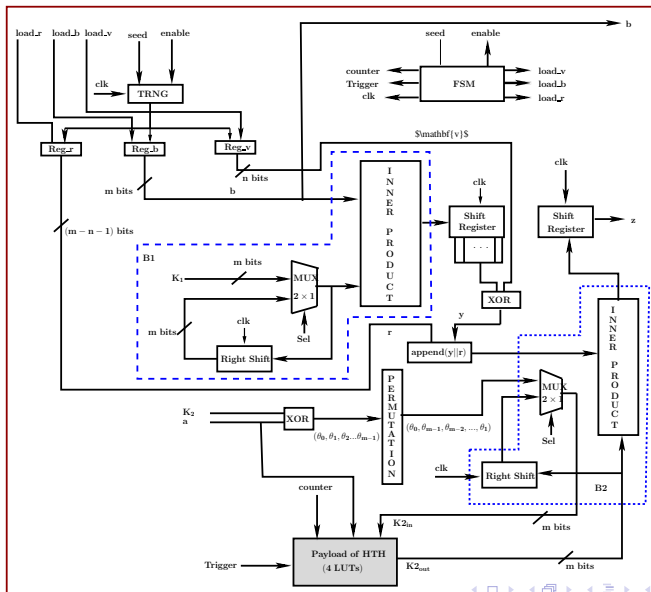
$\theta \in (\epsilon \times n, \frac{n}{2})$  be a threshold value and for 80-bit security,  $m$  is 163 bits

# Tag Impersonation Attack

- The adversary eavesdrops to obtain a triplet  $\mathbf{a}_c, \mathbf{b}_c, \mathbf{z}_c$ .
- $\mathbf{K}_2$  is also known.
- $\mathbf{y}_c = \text{Decode}(\mathbf{z}_c, \mathbf{K}_2 \oplus \mathbf{a}_c)$
- The reader sends  $\mathbf{a}_w$ .
- Adversary reuses  $\mathbf{y}_c$  and calculates  $\mathbf{z}_w = \mathbf{y}_c \cdot C_{\mathbf{K}_2 \oplus \mathbf{a}_w}$  and sends  $\mathbf{z}_w, \mathbf{b}_c$ .
- The reader executes decode algorithm with  $\mathbf{z}_w$  and  $\mathbf{K}_2 \oplus \mathbf{a}_w$  and obtains  $\mathbf{y}_c$  which was already authenticated by the reader for  $\mathbf{b}_c$ .

If the adversary obtains the key  $\mathbf{K}_2$ , it can impersonate as a valid tag, without even having the knowledge of key  $\mathbf{K}_1$ .

# Architecture of LCMQ - Tag



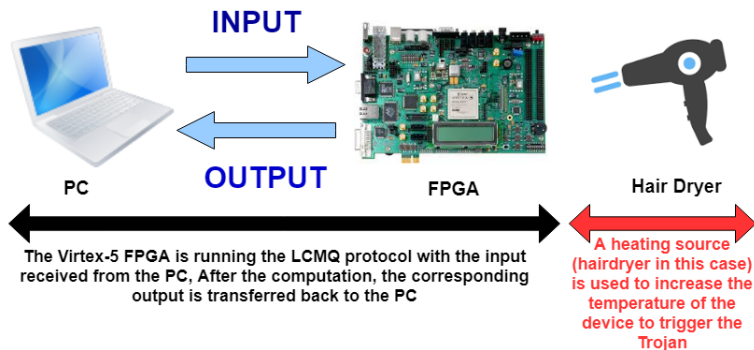
## Adversarial Model:

- The designer is malicious and has a nexus with a personnel at a fabrication facility.
- The personnel in the fabrication facility injects the HTH.
- One must ensure that gate count difference between actual design and infected design should not be very high.
- The HTH is implemented using the LUTs on the FPGAs directly, with almost negligible overhead in power and hardware.

# HTH Induced Safe Error Attack

## Activation:

- External Triggering
- Internal triggering



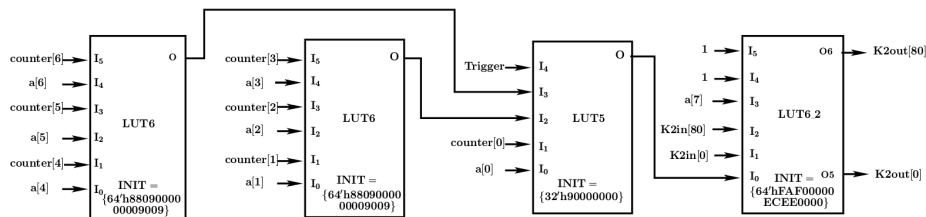
# HTH Induced Safe Error Attack

## Payload:

- We present an ultra-low hardware footprint HTH which occupies only 4 LUTs.
- To obtain  $\mathbf{K}_2$ , we need to inject a fault in all  $m$  bits.
- Exploits the property of circulant matrix to reduce the linear increase in the overhead.

The input key is right shifted at each clock cycle. A stuck at 1 fault induced in the  $1^{\text{st}}$  bit of right shift register in  $t$ -th clock cycle is equivalent in inducing a stuck at 1 fault in  $t$ -th bit of initial input key.

# HTH Induced Safe Error Attack



- 1 **a[6:0] equals counter value and a[7]=0:**  $K_2[0]$  gets injected by the stuck at 1 fault at  $a[6:0]^{th}$  clock cycle. It is equivalent to injecting stuck at one fault at  $a[6:0]^{th}$  bit of  $K_2$ .
- 2 **a[6:0] equals counter value and a[7]=1:**  $K_2[80]$  gets injected by the stuck at 1 fault at  $a[6:0]^{th}$  clock cycle. This injects stuck at one fault at  $(a[6:0]+80)^{th}$  bit of  $K_2$ .

## Advantage of targeting either $K_2[0]$ or $K_2[80]$ :

- To inject fault at  $114^{th}$  bit position, we need to wait 114 cycle.
- If the value of  $a$  is  $162 = 8'b10100100$ ,  $K_2[80]$  can be set as 1 in  $34^{th}$  cycle.
- After inducing the stuck at 1 fault, if the authentication succeeds then the adversary infers that the corresponding bit was 1, otherwise that corresponding bit 0.

# Experimental Setup and Implementation Results

- The hardware designs for both the hardware implementation of the LCMQ protocol and the proposed HTH were performed using *Verilog HDL* and executed on Virtex-5 FPGA board.
- For 80-bit security, the parameter values are:  
 $m = 163, n = 162, \theta = 18, \eta = 0.08$ .
- The designs were synthesized and implemented using *Xilinx ISE 14.5*, and simulated using *Xilinx Isim*.
- The power estimation of the circuit was carried out using *Xilinx XPower Analyzer* and delay estimation using *Xilinx Timing Analyzer*.

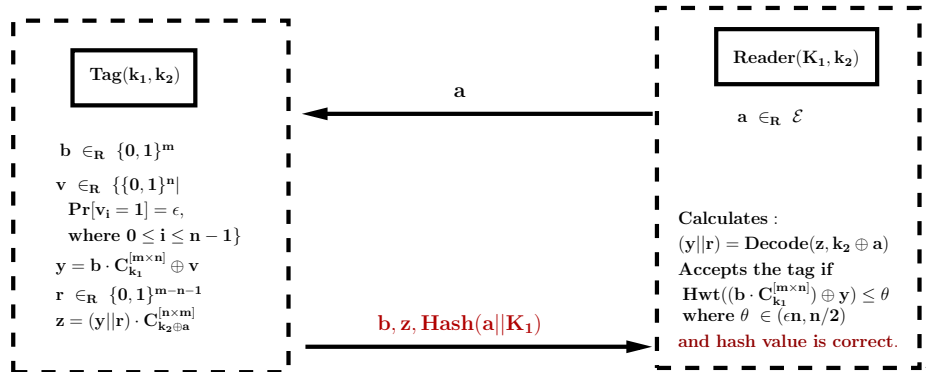
# Experimental Setup and Implementation Results

Table: Power and Execution Time Overhead

Overhead	Original Design	Design with HTH	Increase in Number
Power	0.539 W	0.539 W	0
Timing	3.789 ns	3.794 ns	0.13

Table: Hardware Overhead

Components	Original Design	Design with HTH	Increase in Number
LUT	714	717	0.4
SliceRegs	1507	1507	0
Slices	589	589	0.0



- We made an key observation that in an LCMQ protocol an attacker can impersonate without the knowledge of key  $\mathbf{K}_1$ , thus motivating a HTH designer to just target key  $\mathbf{K}_2$ .
- We gave an effective and efficient architecture of tag part of the LCMQ problem.
- We provided an ultra-lightweight HTH design which can induce safe errors surreptitiously to leak  $\mathbf{K}_2$  potentially.

Thank You