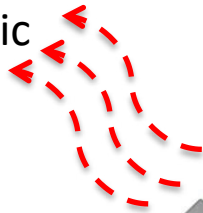


# Automatic Synthesis of Fault Attack Resistant Cipher Implementations

Chester Rebeiro  
IIT Madras

# Side Channel Analysis

Electro magnetic  
Radiation

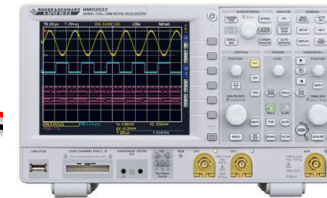


Fault injection

Power consumption



Timing channels



# Preventing Side Channel Attacks is Difficult

overheads

Platform /  
Compiler  
Specific

Programming  
Language  
Specific

**Automatic Synthesis  
of protected implementations**

Naïve implemen  
have signific  
performan

may intro  
Vulnerabilities

Cannot be implemented by  
your average Joe

# Block Cipher Specification Language

```
1.h begin i
2.  h lookups i
3.    SBOX : { 0x63 , 0x7c , 0x77, 0x7b, ... }
4.    KEY  : { 0x54, 0x68, 0x61, 0x74, ... }
5.  h /lookups i
6.  h operations i
7.    h func i h MUL2 ( a ) i
8.      h h : { a : RS ( a , 7 ) } i
9.      h t : { a : LS ( a , 1 ) } i
10.     h n : { h : MUL ( h , 0x1b0 ) } i
11.     h m : { ( n , t ) : XOR ( n , t ) } i
12.     ret m
13.   h / func i
14.   .....
15. h /operations i
16. .....
17. h F2 i h nonlinear i h SUBBYTE i h
18.   h F2[1] : { F1[1] : LKUP ( F1[1], SBOX ) } i
19.   .....
20.   h F2[16] : { F1[16] : LKUP ( F1[16], SBOX ) } i
21. /i
22. h F3 i h linear i h PERMUTE i h
23.   h F3[1] : { F2[1] } i
24.   .....
25.   h F3[16] : { F2[12] } i
26. /i
27. h F4 i h linear i h MDS i h
28.   h F4[1] : { ( F3[1], F3[2], F3[3], F3[4] ) :
29.     XOR ( XOR ( MUL2 ( F3[1] ), MUL3 ( F3[2] ) ), XOR ( F3[3], F3[4] ) ) } i
30.   .....
31.   h F4[16] : { ( F3[13], F3[14], F3[15], F3[16] ) :
32.     XOR ( XOR ( MUL2 ( F3[16] ), MUL3 ( F3[23] ) ), XOR ( F3[14], F3[15] ) ) } i
33.h end i
```

HTML like language that captures basic functionality of the cipher

- operations
- information flow

Just need one per cipher  
Platform independent  
Programming language independent

# Synthesis Tools

Source Code  
(Java / Assembly / RTL)

## Synthesis tools

```
1: h begin i
2:   h lookups i
3:     SBOX: { 0x63, 0x7c, 0x77, 0x7b, ... }
4:     KEY: { 0x64, 0x68, 0x61, 0x74, ... }
5:   h /lookups i
6:   h operations i
7:     h func i h MUL2 (a) i
8:       h n: { a: RS (a, 7) } i
9:       h t: { a: LS (a, 1) } i
10:      h n: { n: MUL (n, 0x10) } i
11:      h m: { (n, t): XOR (n, t) } i
12:      ret m
13:    h /func i
14:  h /operations i
15:  h F2 i h nonlinear i h SUBBYTE i h
16:    h F2[1]: { F_1[1]: LKUP (F_1[1], SBOX) } i
17:    h F2[16]: { F_1[16]: LKUP (F_1[16], SBOX) } i
18:  h F3 i h linear i h PERMUTE i h
19:    h F3[1]: { F2[1] } i
20:    h F3[16]: { F2[12] } i
21:  h F4 i h linear i h MCS i h
22:    h F4[1]: { (F_3[1], F_3[2], F_3[3], F_3[4]):
23:      XOR (XOR (MUL2 (F_3[1]), MUL3 (F_3[2])), XOR (F_3[3], F_3[4])) } i
24:    h F4[16]: { (F_3[13], F_3[14], F_3[15], F_3[16]):
25:      XOR (XOR (MUL2 (F_3[16]), MUL3 (F_3[23])), XOR (F_3[14], F_3[15])) } i
26:  h /
27:  h end i
28: 33: h end i
```

Specification

Side-Channel  
Evaluation  
&  
Synthesis

```
uint8_t F1[16], F2[16], F2d[16];
uint8_t SBOX[256] = {S1, S2, ..., S256};

F2[0] = SBOX[F1[0]];
F2[1] = SBOX[F1[1]];
...
F2[15] = SBOX[F1[15]];

F2d[0] = SBOX[F1[0]];
F2d[1] = SBOX[F1[1]];
...
F2d[15] = SBOX[F1[15]];

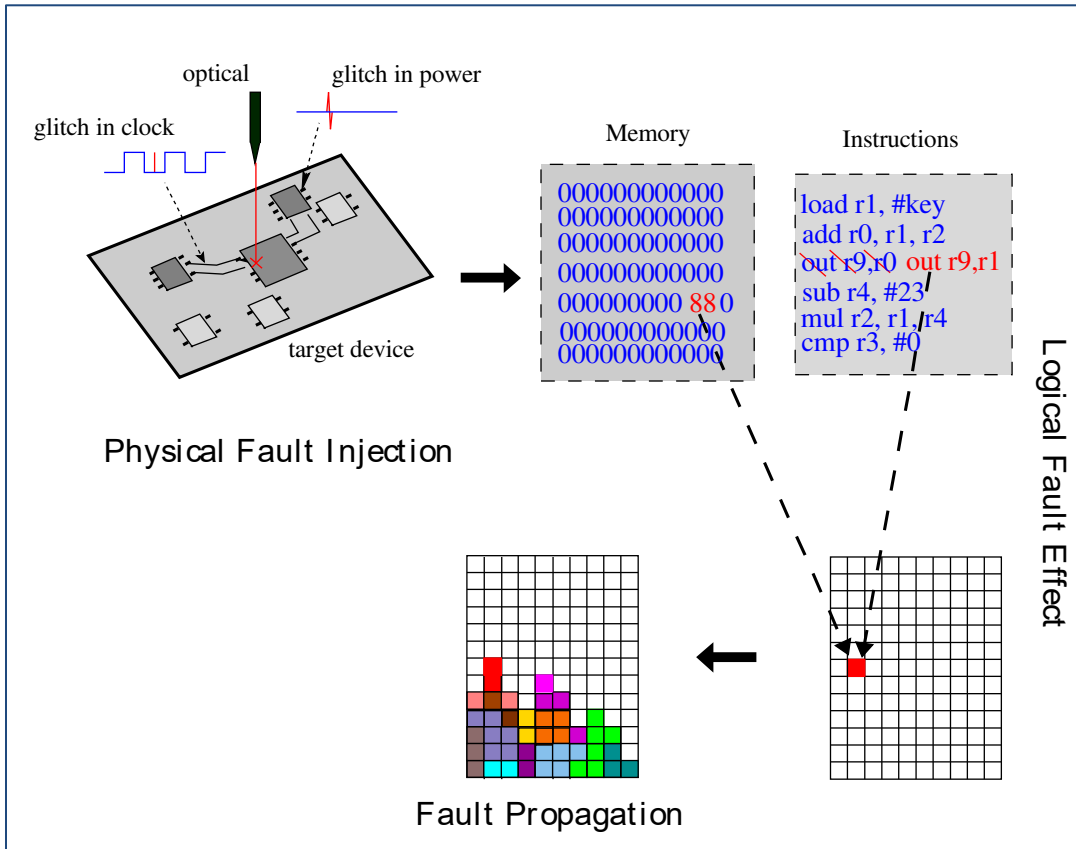
if (F2[0] == F2d[0] && ... && F2[15] == F2d[15])
{
    continue;
}
else
{
    exit(0);
}
```

compiler

Side-channel secure  
Executable / design

# Automatic Synthesis of Fault Attack Resistant Block Cipher Implementations

# Fault Injection in Block Ciphers

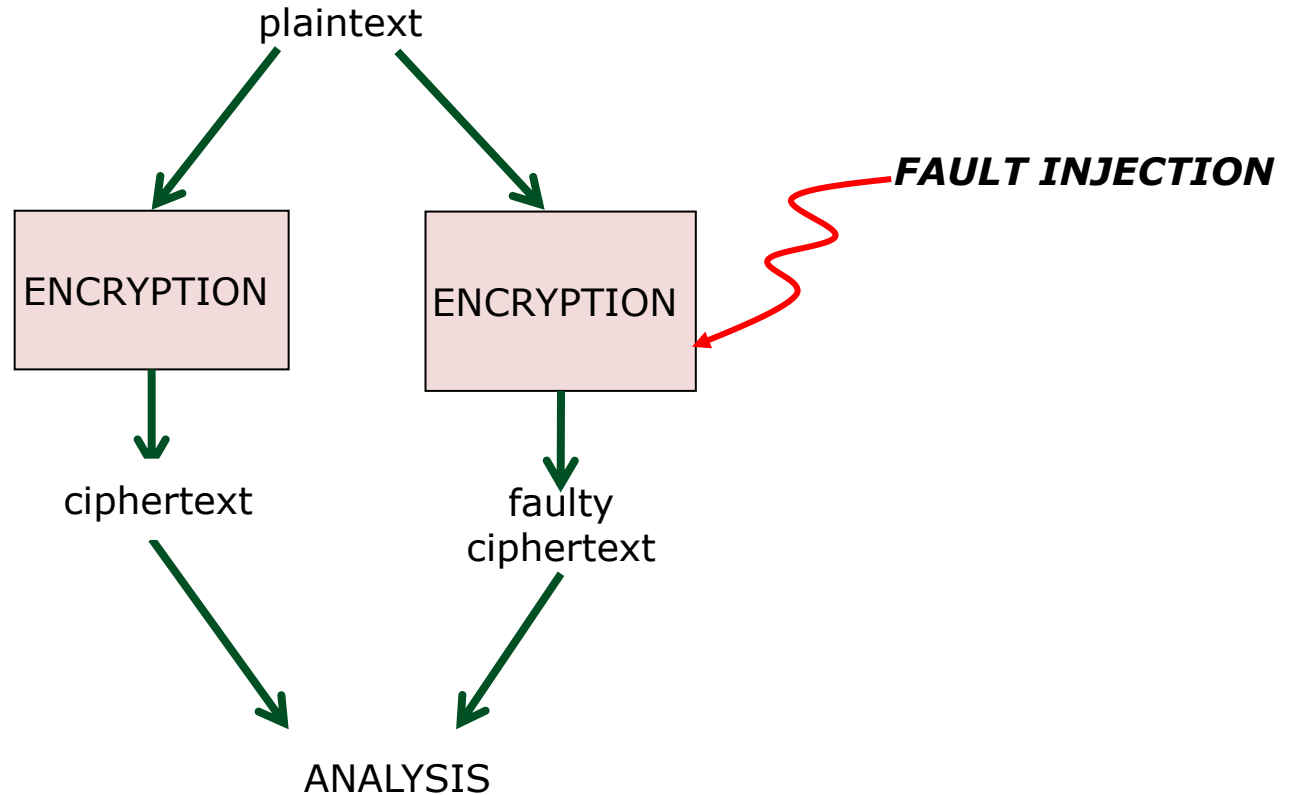


Random single byte fault injection

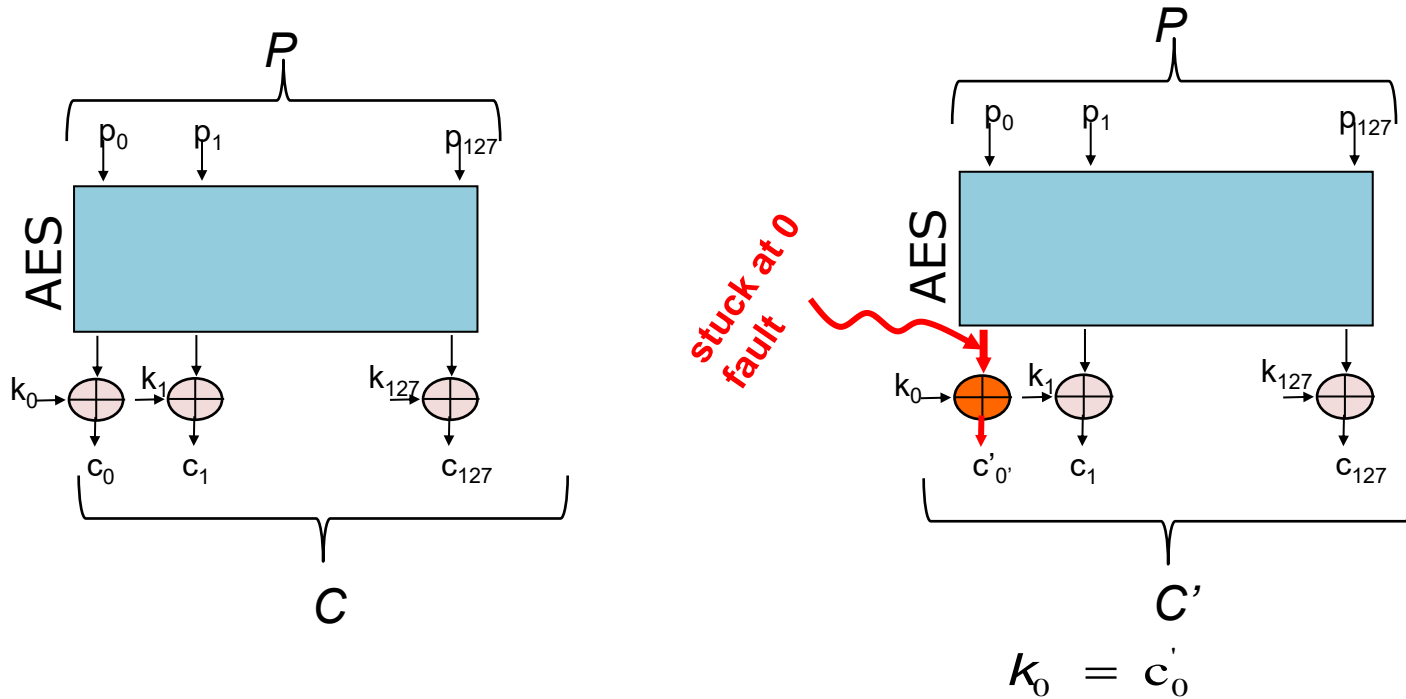
Logical Fault Effect

Fault Propagation

# Differential Fault Attacks



# A Simple AES Fault Attack



Many more stronger fault attacks are possible

# Central Idea in DFA

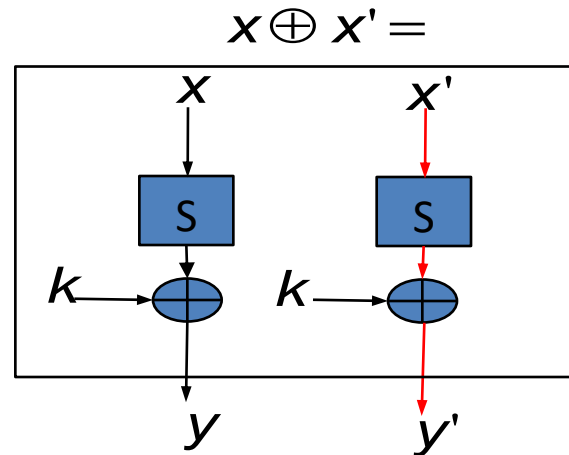
Fault attackers look to solve equations in one of the following form

$$S^{-1}(y \oplus k) \oplus S^{-1}(y' \oplus k) =$$

where  $x$  and  $x'$  are known and  $k$  and  $y$  are unknown.

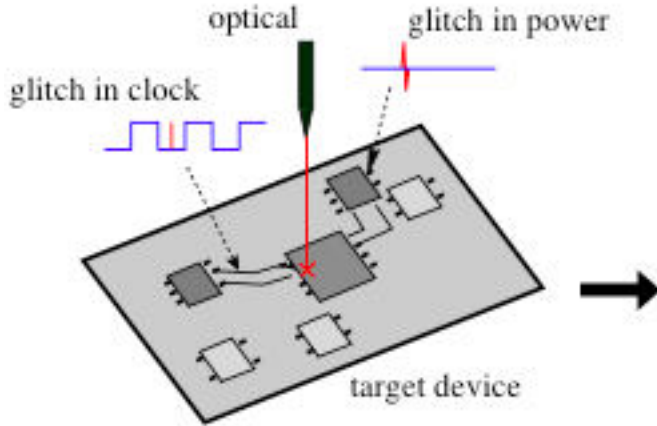
Iterate over all possible values of  $k$  and identify those that satisfy the above equations.

The number of solutions depends on the properties of the S-box.





# summarize



**Inject Fault**

Involving sbox

Linear functions

$$\begin{aligned} S^{-1}(y_1 \oplus k_1) \oplus S^{-1}(y'_1 \oplus k_1) &= g_1(\delta) \\ S^{-1}(y_2 \oplus k_2) \oplus S^{-1}(y'_2 \oplus k_2) &= g_2(\delta) \\ \vdots & \\ S^{-1}(y_n \oplus k_n) \oplus S^{-1}(y'_n \oplus k_n) &= g_n(\delta) \end{aligned}$$

More the better

**Solve Equations**

Online complexity : #faults are needed to retrieve the key

Offline complexity : Search space for finding the keys

# Differential Fault Attacks on AES

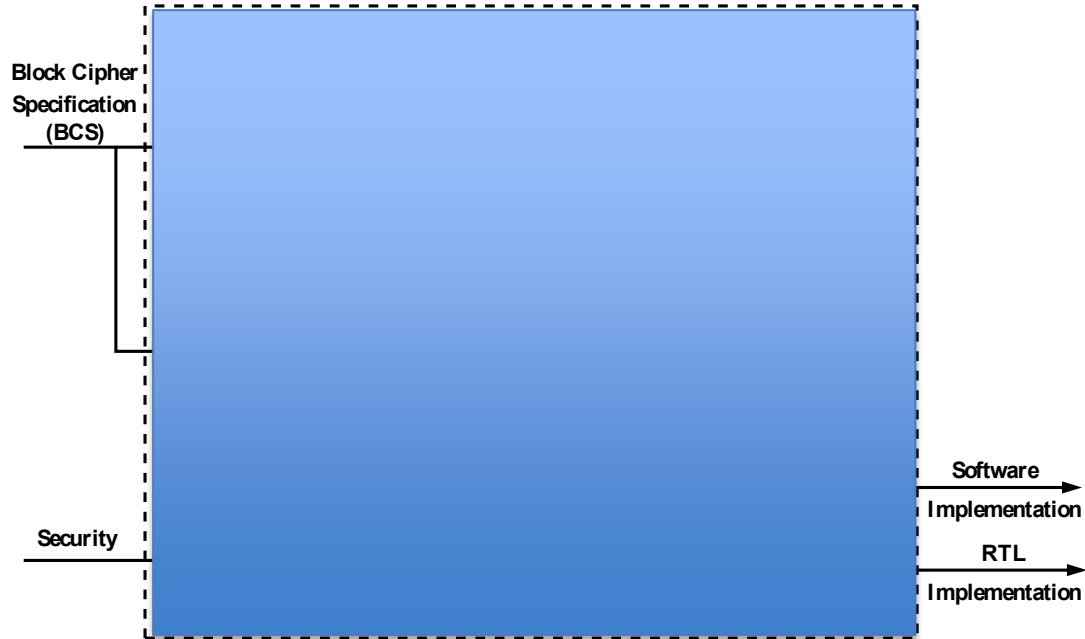
Fault Injected	#faults (online complexity)	Offline complexity
in first round	requires 128 faults	NIL
in last round	requires 128 faults	NIL
in 9 <sup>th</sup> round	requires 4 faults (each fault derives 32 bits of key)	256
in 8 <sup>th</sup> round	Requires 1 fault	256
all other rounds	Not exploitable	N/A

A majority of the faults are unexploitable

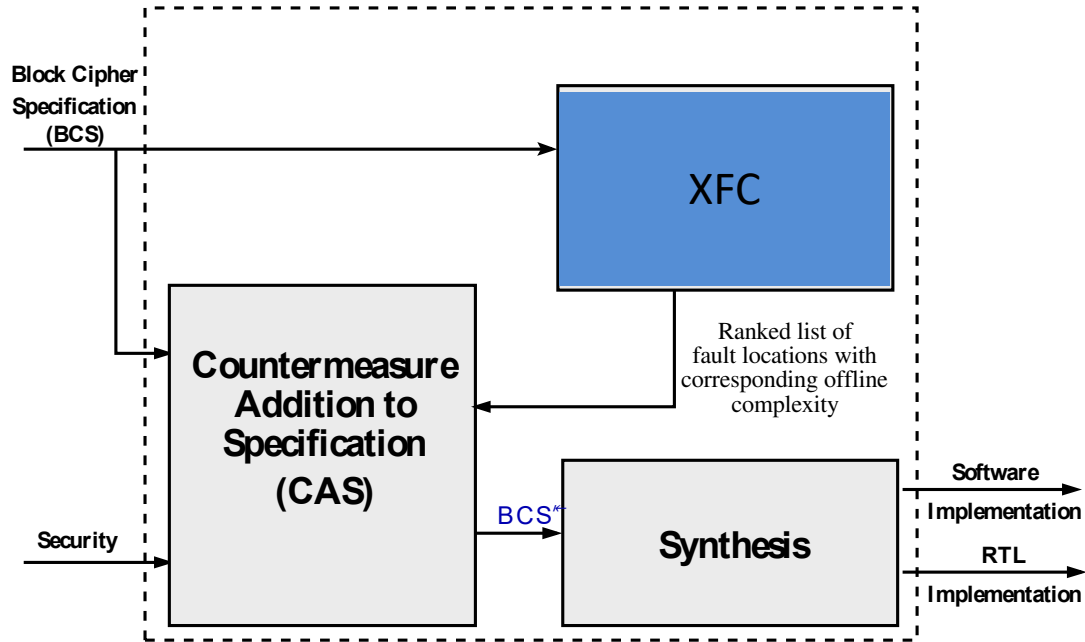
Naïve countermeasures do not consider the online or offline attack complexity requirements, thus significant overheads

# SAFARI

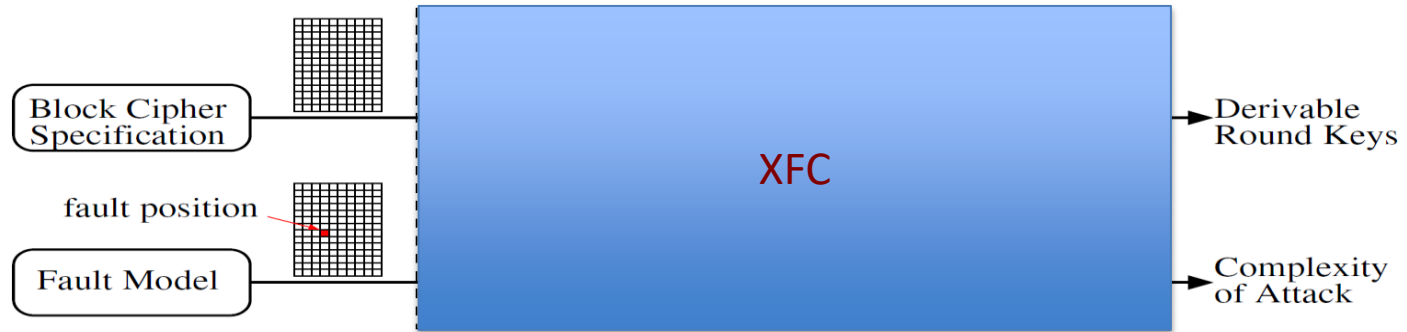
Automatic Synthesis of Fault Attack Resistant Block Cipher Implementations



# XFC: Exploitable Fault Characterization

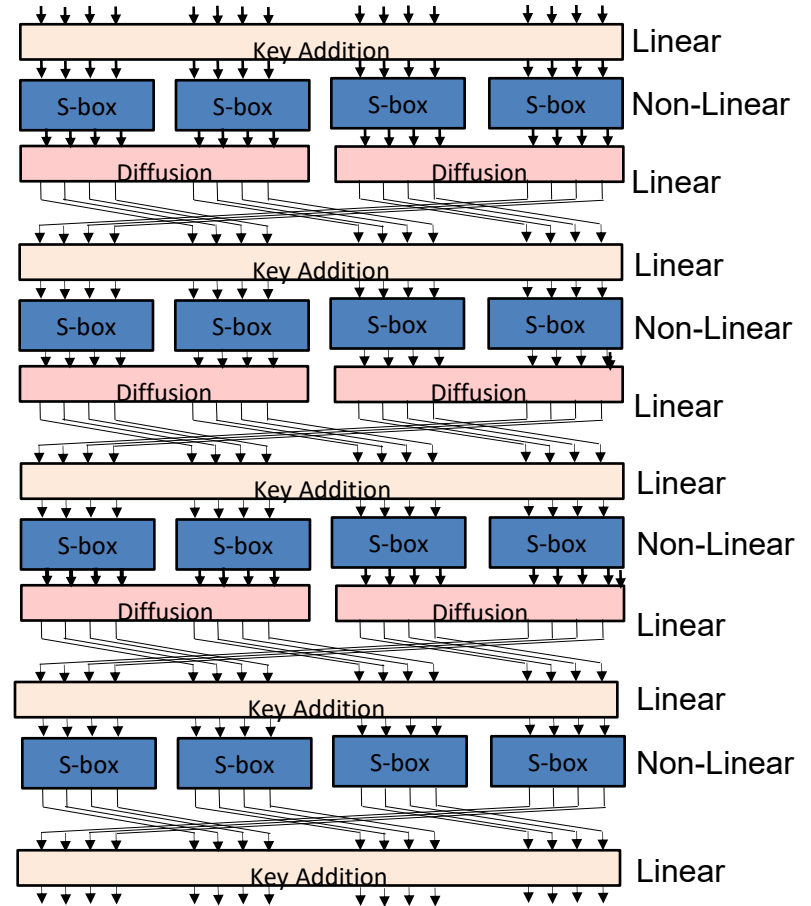


# XFC



# Fault Propagation Phase

A Typical Block Cipher

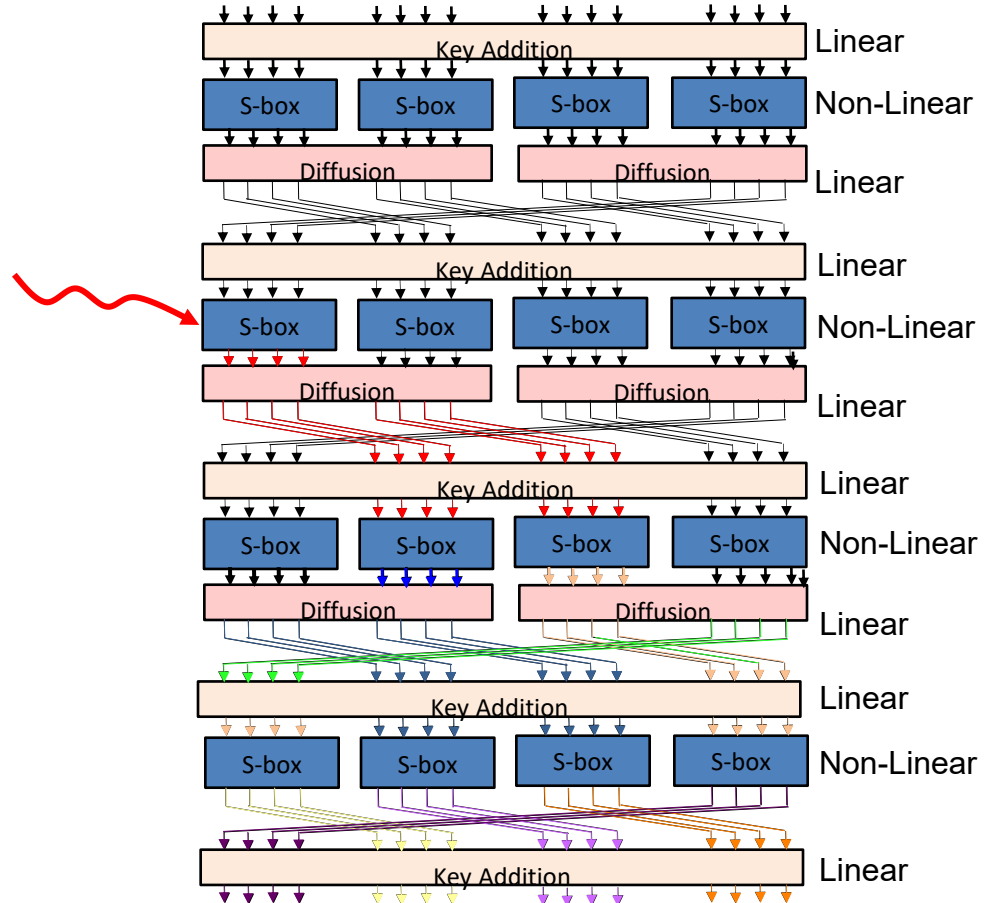


# Fault Propagation Phase

Color the fault affected part.  
Propagate and color as follows.

1. When passing through a linear layer, retain same color
2. When passing through a non-linear layer, change color
1. If two bytes of different colors are combined, change the color.

Same colors are linearly correlated  
Different colors are not correlated



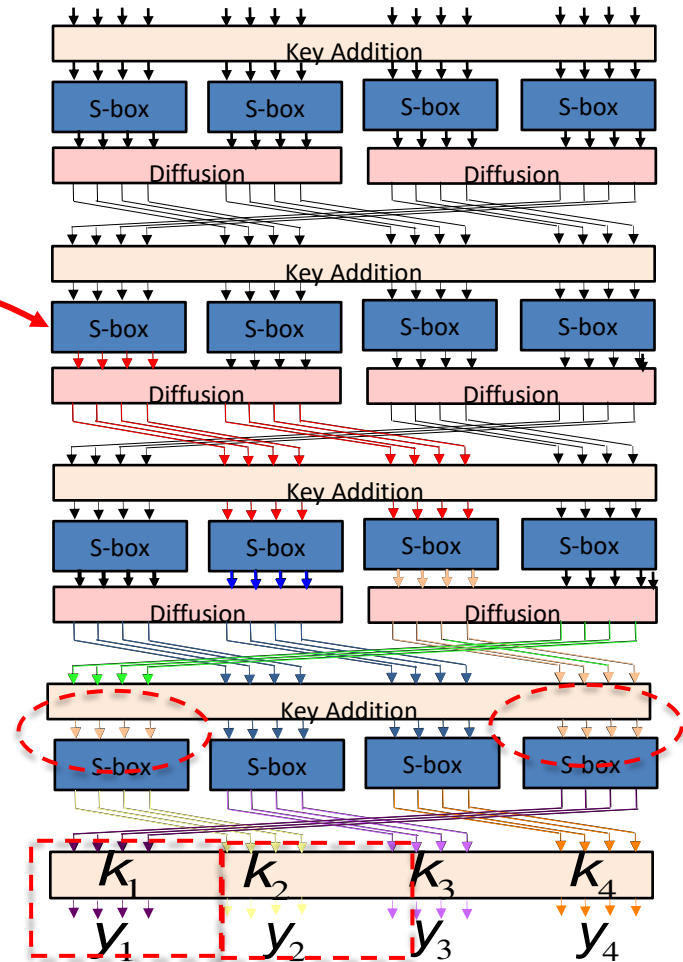
# Key Determination Phase

$$S^{-1}(y_1 \oplus k_1) \oplus S^{-1}(y_1' \oplus k_1) = g_1(\cdot)$$

$$S^{-1}(y_2 \oplus k_2) \oplus S^{-1}(y_2' \oplus k_2) = g_2(\cdot)$$

For every possible value of  
determine  $k_1$ ,  $k_2$  that satisfy the equations.

The complexity is  $2^4$ ; the possible  
values can take.

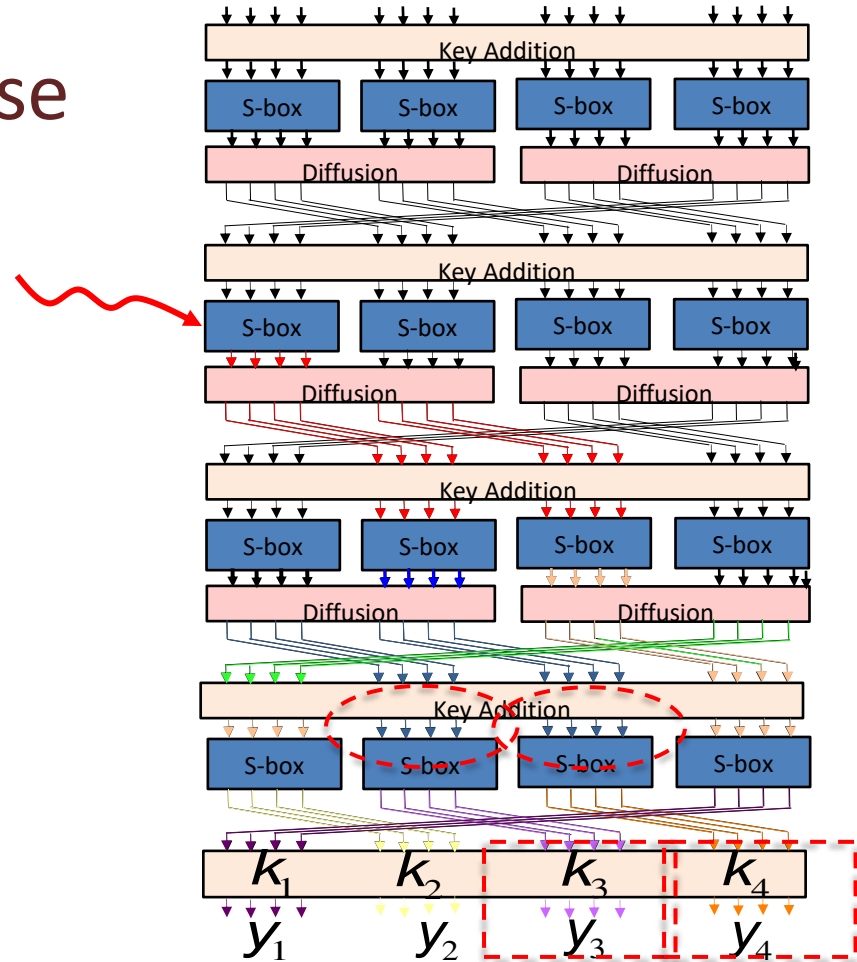


# Key Determination Phase

$$S^{-1}(y_3 \oplus k_3) \oplus S^{-1}(y_3' \oplus k_3) = g_3(\ )$$

$$S^{-1}(y_4 \oplus k_4) \oplus S^{-1}(y_4' \oplus k_4) = g_4(\ )$$

Can be used to determine  $(k_3, k_4)$

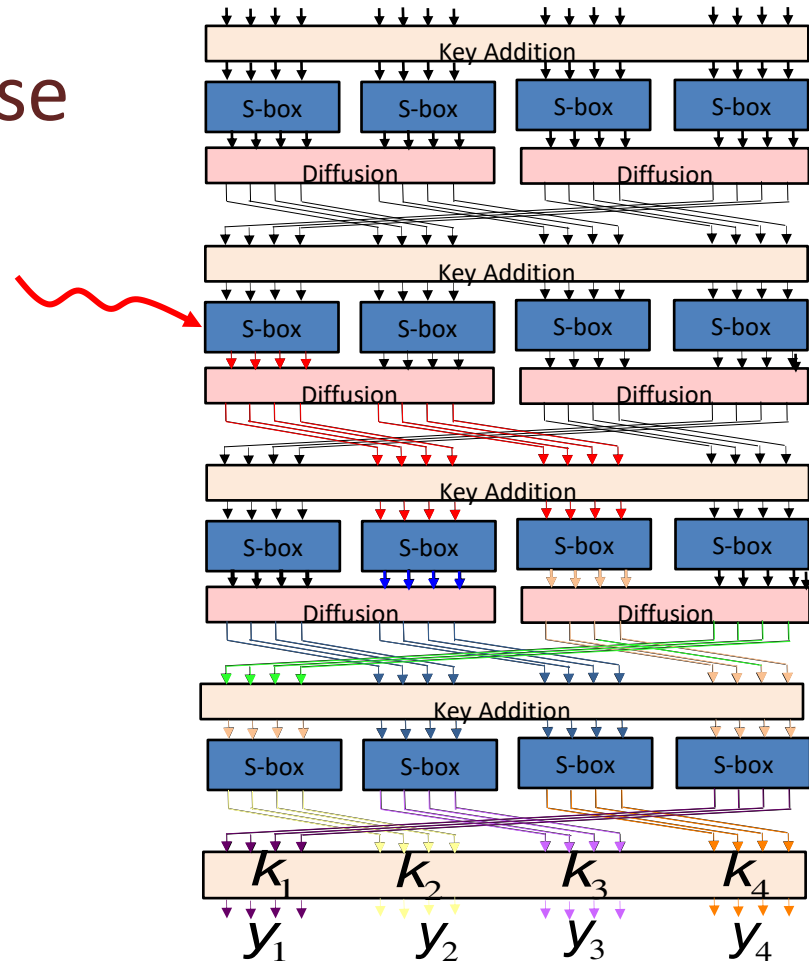


# Key Determination Phase

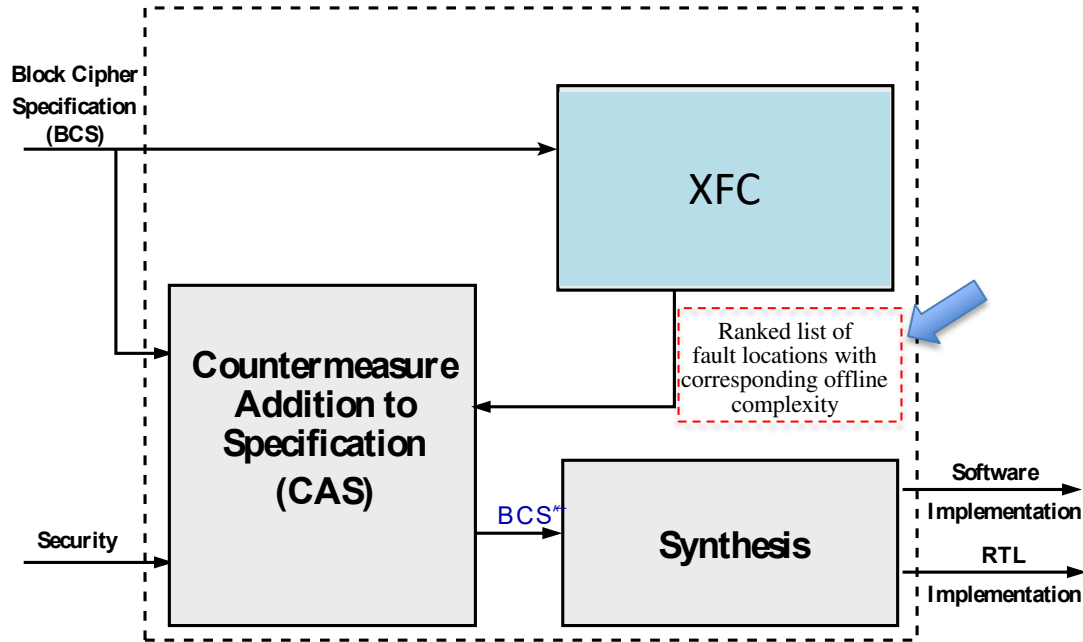
We can thus determine keys  $(k_1, k_2, k_3, k_4)$  and, based on the S-Box properties, we can compute the offline complexity

Continue this process upwards toward the location of the fault eventually getting a result  
As follows:

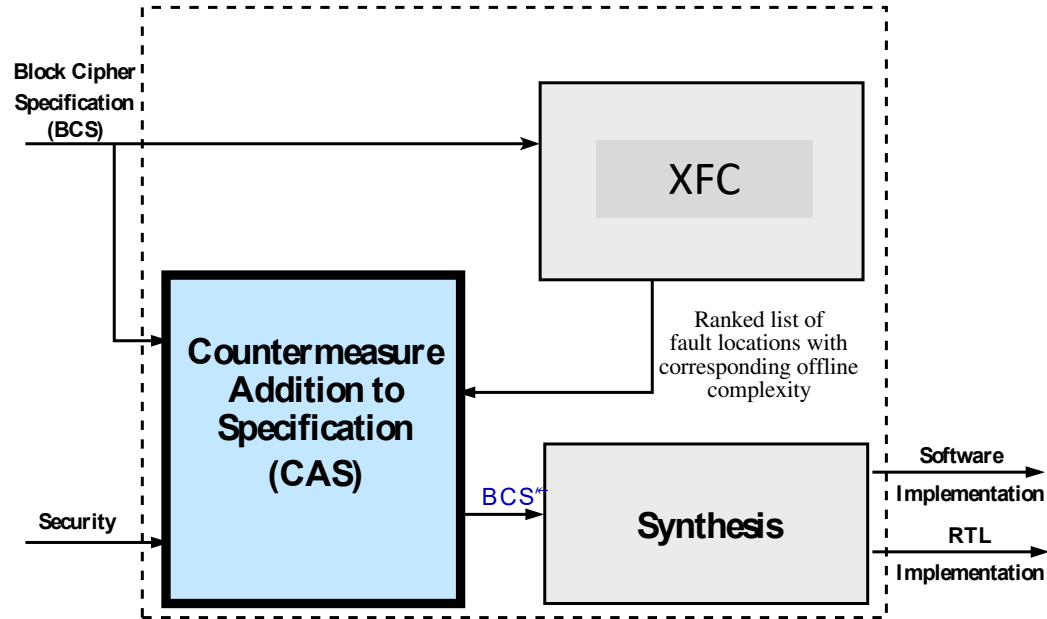
Fault at location  $x$  gives keys  $(k_1, k_2, k_3, k_4)$  with an offline complexity of



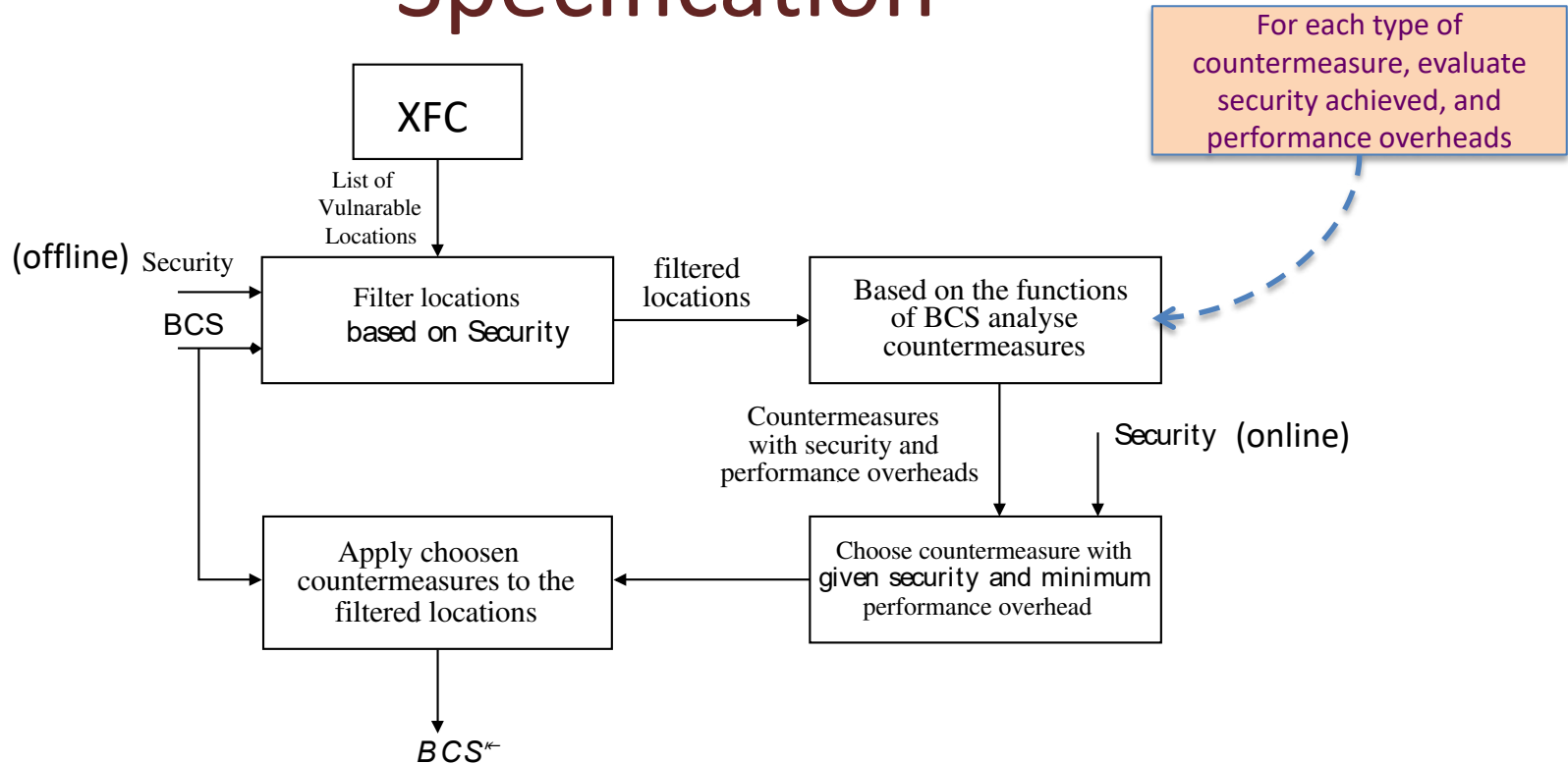
# XFC: Exploitable Fault Characterization



# Countermeasure Addition to Specification



# Countermeasure Addition to Specification



# Analysis of Redundancy

## Security Analysis

If the probability of injecting a fault  $f$  is  $p_f$ , then the probability with which an attack is successful ( $p_s$ ) is defined as :

$$p_s = \prod_{i=1}^{55} p_f \rightarrow p_f = \prod_{i=1}^{55} p_f^2 .$$

## Performance Overhead

- Overhead is estimated in terms of time and area from  $BCS^{\leftarrow}$ .
- For Software synthesis, number of extra clock cycles required is calculated.
- If the target device is known then we know the number of clock cycles taken by each of the primitive operations. Hence total time can be estimated
- For Hardware synthesis overhead estimated through number of extra gates used.

# Countermeasure Evaluation

## For Software

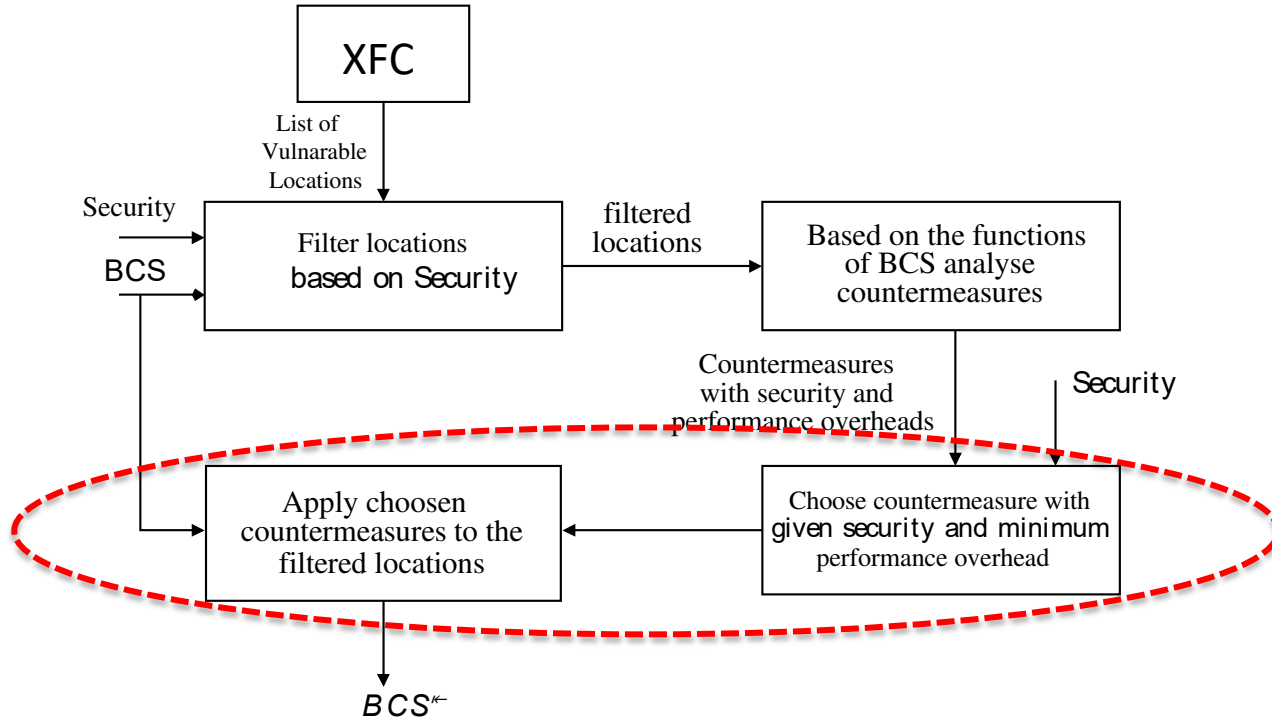
Countermeasures	Security	Function	Memory Overhead (in bytes)	$T_e$	Memory $\rightarrow T_e$
Redundancy	1/255	ARK	64	96	6144
	1/255	SB	256	64	16384
	1/255	MC	-	400	400
1 Bit Parity	1/2	ARK	-	256	256
	1/2	SB	32	256	8192
	63/255	MC	-	448	448
2 Bit Parity	1/4	ARK	-	288	228
	1/4	SB	64	272	17409
	15/255	MC	-	960	960
4 Bit Parity	1/16	ARK	-	192	192
	1/16	SB	128	224	28672
	1/255	MC	-	976	976

# Countermeasure Evaluation

## For Hardware

Countermeasure	Security	Function	XOR	AND	OR	Others
Redundancy	1/ 255	ARK	256	0	128	16, 8 Bit Register
	1/ 255	SB	128	0	128	8 Bit 256 → 1 MUX
	1/ 255	MC	768	0	128	-
1 Bit Parity	1/ 2	ARC	128	16	15	-
	1/ 2	SB	128	16	15	8 Bit 16 → 1 MUX
	63/ 255	MC	176	16	15	-
2 Bit Parity	1/ 4	ARC	128	32	31	-
	1/ 4	SB	128	32	31	8 Bit 32 → 1 MUX
	15/ 255	MC	432	32	31	-
4 Bit Parity	1/ 16	ARK	128	64	63	-
	1/ 26	SB	128	64	63	8 Bit 64 → 1 MUX
	1/ 255	MC	608	64	63	-

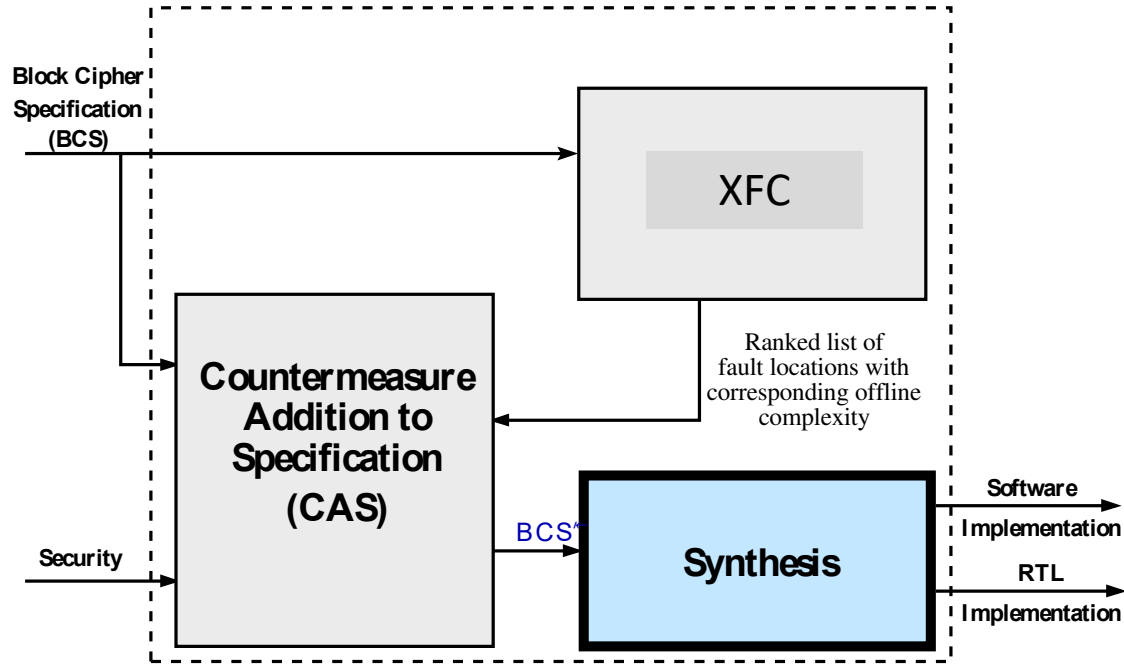
# Countermeasure Addition to Specification



# Modified Block Cipher Specification

```
h F2i h nonlinear i h SUBBYTE i h
  h F2[1] : { F1[1] : LKUP ( F1[1], SBOX ) } i
  h F2[2] : { F1[2] : LKUP ( F1[2], SBOX ) } i
  .....
  h F2[16] : { F1[16] : LKUP ( F1[16], SBOX ) } i
/i
//Adding redundant computation of F2
h F2k i h nonlinear i h SUBBYTE i h
  h F2k[1] : { F1[1] : LKUP ( F1[1], SBOXd ) } i
  h F2k[2] : { F1[2] : LKUP ( F1[2], SBOXd ) } i
  .....
  h F2k[16] : { F1[16] : LKUP ( F1[16], SBOXd ) } i
/i
//Adding function to compare results of original and redundant function
h F2d i h linear i h CMP i h
  h F2d[1] : { ( F2[1], F2k[1] ) : ECMP ( F2[1], F2k[1] ) } i
  h F2d[2] : { ( F2[2], F2k[2] ) : ECMP ( F2[2], F2k[2] ) } i
  .....
  h F2d[16] : { ( F2[16], F2k[16] ) : ECMP ( F2[16], F2k[16] ) } i
/i
```

# Synthesis



# Synthesis

```
uint8_t F1[16], F2[16], F2d[16];
uint8_t SBOX[256] = {S1, S2, ..., S256};

F2[0] = SBOX[F1[0]];
F2[1] = SBOX[F1[1]];
. . . . .
F2[15] = SBOX[F1[15]];

F2d[0] = SBOX[F1[0]];
F2d[1] = SBOX[F1[1]];
. . . . .
F2d[15] = SBOX[F1[15]];

if (F2[0] == F2d[0] && . . . && F2[15] == F2d[15])
{
    continue;
}
else
{
    exit(0);
}
```

Synthesized C Code(Software)

```
wire[127 : 0] F1, F2, F2d;
wire[15 : 0] F2c;
SubByte SB1 (F1[127 : 120], F2[127 : 120]);
SubByte SB2 (F1[119 : 112], F2[119 : 112]);
. . . . .
SubByte SB16 (F1[7 : 0], F2[7 : 0]);

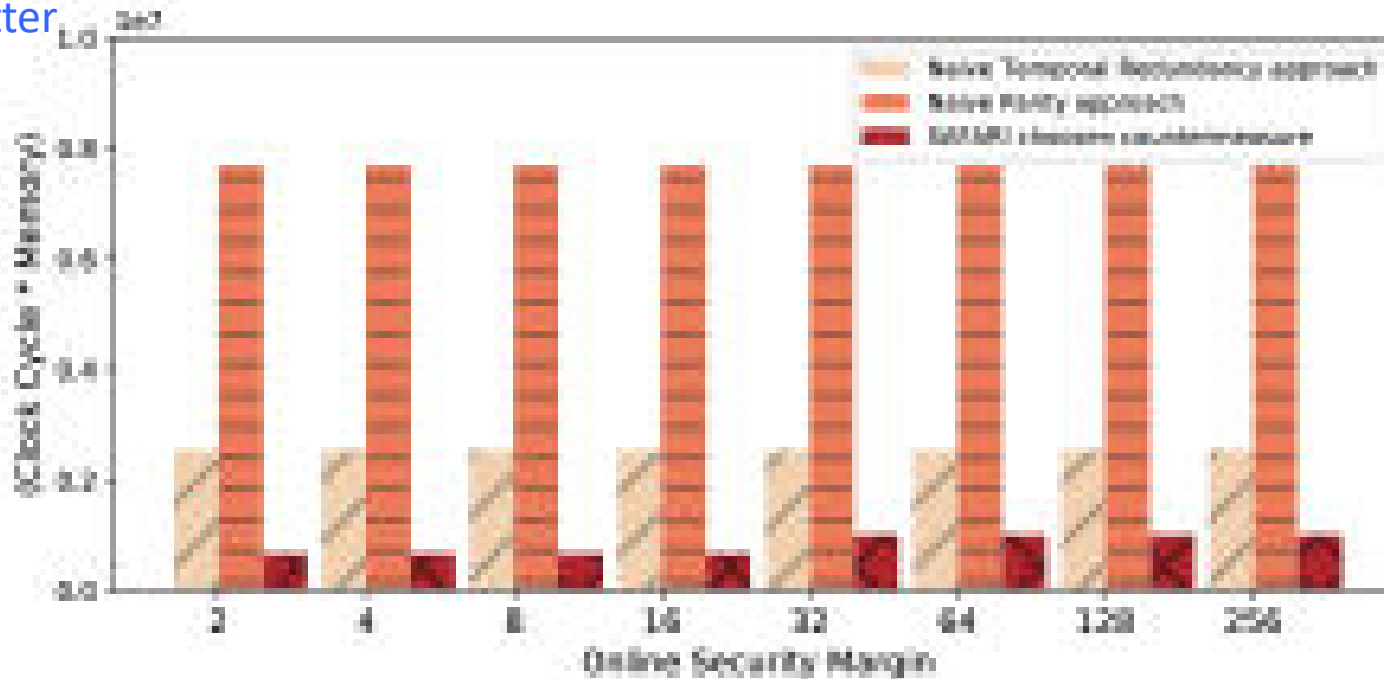
SubByte DSB1 (F1[127 : 120], F2d[127 : 120]);
SubByte DSB2 (F1[119 : 112], F2d[119 : 112]);
. . . . .
SubByte DSB16 (F1[7 : 0], F2d[7 : 0]);

F2c[15] = ECMP(F2[127 : 120], F2d[127 : 120]);
F2c[14] = ECMP(F2[119 : 112], F2d[119 : 112]);
. . . . .
F2c[0] = ECMP(F2[7 : 0], F2d[7 : 0]);
```

Synthesized Verilog Code(Hardware)

# Results (Software)

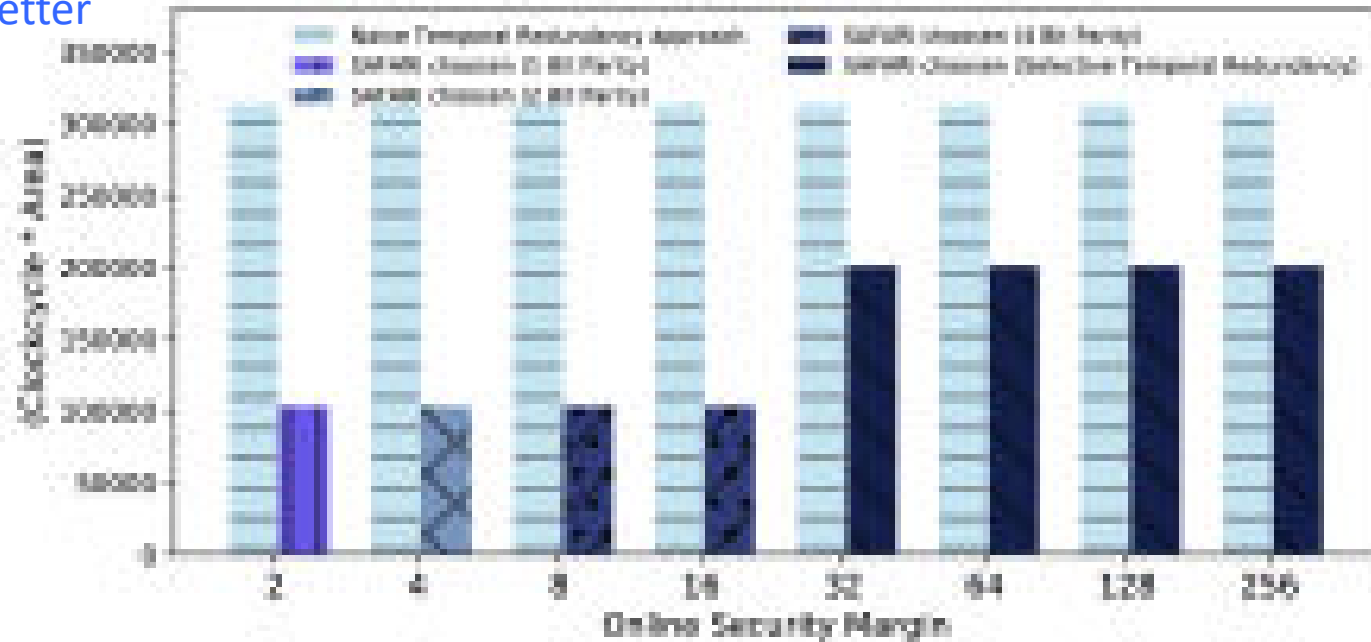
Lower is better



Comparing SAMPAR's generated code with rather manually inserted equivalents that have temporal countermeasures. The comparison is done for an MSP430 processor. The metric used is CLOCK CYCLE \* MEMORY. The results list the average number of fault injections that the code can tolerate.

# Results (Hardware)

Lower is better



Comparing SPARTE's synthesized hardware designs with native manually inserted equivalents that have temporal redundancies. The comparison is done for different security margins for a 20ns ADC. The values on the y-axis is  $CLOCK\ CYCLES * AREA$ . The y-axis has the average number of fault injections that the same can tolerate.

# Conclusions

- First attempt to automatically synthesize fault attack resistant block cipher implementations
  - User configurable security
  - Reduced overheads
  - any block cipher, any device, any programming language
- Covers a wide range of ciphers and countermeasures
- Block Cipher Specification Language
- Limitations:
  - In software especially, the generated code is not very efficient for high performance processors.