INDIAN STATISTICAL INSTITUTE

Periodical Examination

M. Tech (CS) - I Year (Semester - II)

Computer Architecture

Date: 26.02.2009 Maximum Marks: 40 Duration: 2.5 Hours

Note: Be precise in your answers. This is a three page question paper.

Q 1(i): A computer system contains a special purpose processor for doing floating-point operations. You as a designer have determined that 70% of your computations can use the floating-point processor. When a program uses the floating-point processor, the speedup of the floating-point processor is 45% faster than when it does not use it. Find the overall speedup by using the floating-point processor.

Q 1(ii): In order to improve the speedup, you are considering two options:

Option 1: The compiler design is modified so that 80% of the computations can use the floating-point processor. Cost of this option is Rs. 25 lakhs.

Option 2: The floating-point processor is to be modified. The speedup of the floating-point processor is 100% faster than when it does not use it. Assume in this case that 60% of the computations can use the floating point processor. Cost of this option is Rs. 30 lakhs.

Which option would you recommend? Justify your answer quantitatively. [2+4=6]

Q 2: Suppose we make an enhancement to a computer that improves a mode of execution by a factor of 15. The enhanced mode is used 55% of the time measured as a percentage of the execution time when the enhanced mode is in use. Find out (a) what percentage of the original execution time has been converted to fast mode? (b) what is the speedup we have obtained from fast mode? [2+4=6]

Q 3 (i): Describe in short the concept of memory hierarchy explaining the role of each level of memory.

Q 3 (ii): The Clock cycles per instruction (CPI) of a computer system is 3.0 when all memory accesses hit in the cache. The only data accesses are *loads* and *stores* and these total 53%

of the instructions. If the miss penalty is 31 clock cycles and the miss rate is 3%, how much faster would the machine be if all instructions were cache hits? [4+2=6]

Q 4 Consider the following piece of 'C' code.

```
for (i=0; i<= 100; i++)
  {X[i] = Y[i] + Z;}
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Assume that X and Y are arrays of 32-bit integers and C and i are 32-bit integers. Assume that all data values and their addresses are kept in memory at addresses 0, 5000, 1500 and 2000 for A, B, C and i respectively except when they are operated on. Assume that values in registers are lost between iterations of the loop.

(a) Write the code for DLX. (b) How many memory-data references will be executed? (c) What is the code size in bytes? [8+2+1=11]

Q 5: Show how the code sequence $A \times B - (A + C \times B)$ will appear on the following architectures: (a) stack, (b) accumulator, (c) register-memory, and (d) load-store. [1.5+1.5+1.5+1.5=6]

Q 6(i): Explain the effect of instruction pipelining on the bandwidth of the memory systems.

Q 6(ii): Consider an unpipelined machine with five stages (Instruction Fetch, Instruction Decode/Register Fetch, Execute/Address Calculation, Memory Access and Write Back). Assume that it has 11-ns clock cycles. The machine uses four cycles for ALU operations and branches and five cycles for memory operations. Assume that the relative frequencies of these operations are 45%, 15% and 40% respectively. Pipelining the machine adds 1-ns of overhead to the clock. Find out how much speedup we will gain in the instruction execution rate. You can ignore any latency impact. [3+2=5]